Memory, Latches, & Registers

1) Structured Logic Arrays
2) Memory Arrays
3) Transparent Latches
4) Saving a few bucks at toll booths
5) Edge-triggered Registers
General Table Lookup Synthesis

Generalizing:
Remember from a few lectures ago that, in theory, we can build any 1-output combinational logic block with multiplexers.

For an N-input function we need a $2^N$ input multiplexer.

BIG Multiplexers? How about 10-input function? 20-input?
Mux Guts

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Hmmm, by sharing the decoder part of the logic MUXs could be adapted to make lookup tables with any number of outputs.

Multiplexers can be partitioned into two sections.

A decoder that identifies the desired input, and a selector that enables that input onto the output.
A New Combinational Device

DECODER:
k SELECT inputs,
N = 2^k DATA OUTPUTs.
Selected D_j HIGH;
all others LOW.

Now, we are well on our way to building a
general purpose table-lookup device.

We can build a 2-dimensional ARRAY of
decoders and selectors as follows ...
There's an extra level of inversion that isn't necessary in the logic. However, it reduces the "load" on the module driving this one.

This ROM stores 16 bits in 8 words of 2 bits.

We can build a general purpose "table-lookup" device called a Read-Only Memory (ROM), from which we can implement any truth table and, thus, any combinational device.

Made from PREWIRED connections ☐, and CONFIGURABLE connections that can be either connected ● or not connected ☐.
ROM IMPLEMENTATION DETAILS

Hardwired "AND" logic
Programmable "OR" logic

Advantages:
- Very regular design
  (can be entirely automated)

Problems:
- Active Pull-ups
  (Static Power)
- Long metal runs
  (Large Caps)
- Slow

Tiny PFETs with gates tied to ground = resistor pullup that makes wire "1" unless one of the NFET pulldowns is on.

JARGON:
Inputs to a ROM are called ADDRESSES. The decoder's outputs are called WORD LINES, and the outputs lines of the selector are called BIT LINES.


**Logic According to ROMs**

ROMs ignore the structure of combinational functions ...

- Size, layout, and design are independent of function
- Any Truth table can be "programmed" by minor reconfiguration:
  - Metal layer (masked ROMs)
  - Fuses (Field-programmable PROMs)
  - Charge on floating gates (EPROMs)
  - etc.

Model: LOOK UP value of function in truth table...

Inputs: "ADDRESS" of a T.T. entry,

ROM SIZE = # TT entries...

... for an N-input boolean function, size = $2^N \times \#\text{outputs}$
**Example: 7-sided Die**

What nature can’t provide... electronics can (and with the same number of LEDs!).

We want to construct a die with the following sides:

An array of LEDs, labeled as follows, can be used to display the outcome of the die:
Once we’ve written out the truth table we’ve basically finished the design.

Possible optimizations:
- Eliminate redundant outputs
- Addressing tricks
A SIMPLE ROM IMPLEMENTATION

That was Easy!

ROMs are even more flexible than MUXes, because you can design the H/W first, and figure out the logic later!

This is the essence of programmability: "LATE-BINDING" logic specification.
"Programmable" Look-up Tables

Remember, EVERY combinational circuit can be expressed as a lookup table. As a result a ROM is a universal logic device. Unfortunately, the ROMs we’ve built thus far are "HARDWIRED". That is, the function that they compute is encoded by the pull-down transistors that are built into the OR-plane of the ROM. What we’d really like is a combinational gate that could be reconfigured dynamically. For this we’ll need some form of storage.

The function of a ROM is determined by the presence of a transistor at the intersection of a WORD line from the AND array with a BIT line going to the OR array.

How to "store" a "bit"?
**Analog Storage: Using Capacitors**

We’ve chosen to encode information using voltages and we know from physics that we can “store” a voltage as “charge” on a capacitor:

![Diagram of capacitor circuit]

To write:
- Drive bit line, turn on access FET, force storage cap to new voltage

To read:
- precharge bit line, turn on access FET, detect (small) change in bit line voltage

**Pros:**
- compact!

**Cons:**
- it leaks! ⇒ refresh
- complex interface
- reading a bit, destroys it
  (you have to rewrite the value after each read)
- it’s NOT a digital circuit

This storage circuit is the basis for commodity DRAMs
Dynamic Memory

TiN top electrode ($V_{REF}$)

$\text{Ta}_2\text{O}_5$ dielectric

poly word line

access FET

TiN/Ta2O5/W Capacitor

Wordline

0 (µm) 0.6
A “Digital” Storage Element

It’s also easy to build a settable DIGITAL storage element (called a latch) using a MUX and FEEDBACK:

Here’s a feedback path, so it’s no longer a combinational circuit.

“State” signal appears as both input and output.

<table>
<thead>
<tr>
<th>G</th>
<th>D</th>
<th>Q_{IN}</th>
<th>Q_{OUT}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>--</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>--</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>--</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>--</td>
<td>1</td>
</tr>
</tbody>
</table>

Q stable
Q follows \( D \)
A LOOK UNDER THE COVERS

Let's take a quick look at the equivalent circuit for our MUX when the gate is LOW (the feedback path is active)

This storage circuit is the basis for commodity SRAMs

Advantages:
1) Maintains remembered state for as long as power is applied.
2) State is DIGITAL

Disadvantage:
1) Requires more transistors
**Why Does Feedback = Storage?**

**BIG IDEA:** use positive feedback to maintain storage indefinitely. Our logic gates are built to restore marginal signal levels, so noise shouldn’t be a problem!

![Diagram of feedback system](image)

**Result:** a bistable storage element

**Feedback constraint:** $V_{\text{IN}} = V_{\text{OUT}}$

**VTC for inverter pair**

**Three solutions:**
- two end-points are stable
- middle point is unstable

We’ll get back to this!
**Static D Latch**

Positive latch:
- D  Q  
- G  

Q follows D

Q stable

Negative latch:
- D  Q  
- G  

"static" means latch will hold data (i.e., value of Q) while G is inactive, however long that may be.

What is the difference?
Design of sequential circuits MUST guarantee that inputs to sequential devices are valid and stable during periods when they may influence state changes. This is assured with additional timing specifications.

**A DYNAMIC DISCIPLINE**

- **t\_PULSE**: minimum pulse width
  - guarantee $G$ is active for long enough for latch to capture data

- **t\_SETUP**: setup time
  - guarantee that $D$ value has propagated through feedback path before latch closes

- **t\_HOLD**: hold time
  - guarantee latch is closed and $Q$ is stable before allowing $D$ to change

- **t\_CD**: minimum contamination delay
  - the soonest that an output will change in response to an input changing

- **t\_PD**: maximum propagation delay
  - the latest that an output will become valid in response to an input changing

If $t\_cd$ isn't provided, you can safely assume it is 0.
**Storage alone is not enough!**

We need to open the gate long enough to capture the output of the ROM, but no so long that it the ROM responds to its new input before the gate closes. Opening gates is tricky!

 Hmm. Hard to get pulse width exactly right!
Here's a strategy for saving 2 bucks the next time you find yourself at a toll booth!
**Escapement Strategy**

The Solution:
Add two gates and only open one at a time.
(Psst... Don’t tell the toll folks)

KEY: At no time is there an open path through both gates...
Edge-triggered Flip Flop

logical "escapement"

Observations:

- only one latch "transparent" at any time
- master closed when slave is open (CLK is high)
- slave closed when master is open (CLK is low)
- no combinational path through flip flop
- Q only changes shortly after 0→1 transition of CLK, so flip flop appears to be "triggered" by rising edge of CLK

Transitions mark instants, not intervals
Flip-flop Timing

D → D

master
G

slave
G

D → Q

Q → D

CLK

master closed
slave open

slave closed
master open
Two Issues

- Must allow time for the input’s value to propagate to the Master’s output while CLK is LOW.
  - This is called "SET-UP" time (How long a D input must valid before the clock rises)
- Must keep the input stable, just after CLK transitions to HIGH. This is insurance in case the SLAVE’s gate opens just before the MASTER’s gate closes.
  - This is called "HOLD-TIME" (How long a D input must "remain" valid after the clock rises)
  - Can be zero (or even negative!)
- Assuring "set-up" and "hold" times is what limits a computer’s performance
**Flip-Flop Timing Specs**

\[ \text{Q} \quad \text{CLK} \quad \text{D} \quad \text{Q} \]

\[ \text{CLK} \quad \text{D} \quad \text{Q} \quad \text{Q} \]

\[ \text{D} \quad \text{Q} \quad \text{Q} \quad \text{CLK} \]

- **\( t_{PD} \):** maximum propagation delay, \( \text{CLK} \rightarrow \text{Q} \)
- **\( t_{SETUP} \):** setup time
  
  *guarantee that D has propagated through feedback path before master closes*

- **\( t_{HOLD} \):** hold time
  
  *guarantee master is closed and data is stable before allowing D to change*
**SUMMARY**

- Regular Arrays can be used to implement arbitrary logic functions
- ROMs decode every input combination (fixed-AND array) and compute the output for it (customized-OR array)
- Memories
  - ROMs are HARDWIRED memories
  - RAMs include storage elements at each WORD-line and BIT-line intersection
    - dynamic memory: compact, only reliable short-term
    - static memory: controlled use of positive feedback
- Level-sensitive D-latches for static storage
- Dynamic discipline (setup and hold times)